What Is Claimed Is:

1. A method for selecting one of a plurality of paths for achieving a data processing result in data processing with at least possible use of multidimensional fields of configurable data handling elements,
wherein characterizing variables based on power consumption are assigned to the data handling elements as a function of the configuration, a path selection being made with an evaluation of the assignment.

2. The method as recited in the preceding claim,
wherein one of a plurality of different algorithms is selected.

3. The method as recited in the preceding independent claim or a subclaim thereto,
wherein one of a plurality of different configurations is selected.

4. The method as recited in the preceding independent claim or a subclaim thereto,
wherein, when selecting a path, a decision is made regarding the assignment of a given data processing task and/or subtask to a multidimensional field of configurable data handling elements and/or another data processing architecture, in particular to an ASIC and/or to a CPU that operates purely sequentially.

5. The method as recited in the preceding independent claim or a subclaim thereto,
wherein a two-dimensional field of configurable data handling elements is considered.

6. The method as recited in the preceding independent claim or a subclaim thereto,
wherein a selection is made from a runtime configurable

processor field, which is partially reconfigurable without interference in particular.

7. The method as recited in the preceding independent claim or a subclaim thereto,
wherein at least some, preferably all of the elements, namely buses, registers, ALUs, RAMs and/or other coarsely granular data handling elements are considered as configurable data handling elements.

8. The method as recited in the preceding independent claim or a subclaim thereto,
wherein the characterizing value is selected independently of the actual task currently being assigned and is selected only as a function of whether or not the particular data handling element is used at all.

9. The method as recited in the preceding claim,
wherein a unique code number is assigned to each configuration being used.

10. The method as recited in the preceding independent claim or a subclaim thereto,
wherein a variable based on electric current, work and/or power is assigned as the variable characteristic of consumption.

11. The method as recited in the preceding claim,
wherein a selection is made, taking into account a cumulative value of variables characteristic of consumption.

12. The method as recited in the preceding independent claim or a subclaim thereto,
wherein a selection is made taking into account additional variables, in particular a required execution time and/or required resources, a momentary processor

utilization and/or a momentarily desired and/or possible power consumption.

13. The method as recited in the preceding claim, wherein a selection is made before the actual data processing.

14. The method as recited in the preceding independent claim or a subclaim thereto, wherein the characterizing variables are supplied and/or selected in simulation of data processing.

15. The method as recited in the preceding independent claim or a subclaim thereto, wherein a selection is made during runtime.

16. A method for operating a multidimensional field of reconfigurable elements, systems of groups of elements handling data together being configured into the field in a predetermined manner during runtime for processing of predetermined tasks,
wherein for at least one task to be processed, a plurality of such element group systems in the multidimensional field suitable for processing the predetermined task is determined;
a particularly suitable element group system is then selected from the plurality for processing the predetermined task; and
the selected one is configured into the field.

17. The method as recited in the preceding claim, wherein the element group system is selected on the basis of its geometry in comparison with the geometry in the field of elements already available for reconfiguration and/or presumably soon to be available.

18. The method as recited in the preceding independent claim or a subclaim thereto, in which configuration data pertaining to element group systems is input from a memory having non-negligible access times and/or is generated with non-negligible generation times, wherein at least for some configurations, at first only a characteristic data record that is reduced in size in comparison with the configuration data record of all configuration data, in particular a characteristic data record pertaining to the geometry, is input into an element group system selection stage, a selection is made on the basis of the characteristic data record and then the configuration data is read from the memory or generated in response to this selection.

19. The method as recited in the preceding independent claim or a subclaim thereto,
wherein data handling elements are configured into the field in a predetermined manner during runtime for processing of predetermined tasks in reconfiguration of the field for performing a plurality of tasks to be executed at least to some extent simultaneously, of which data handling elements are configured into the field for at least two groups together; a plurality of such element group systems which are suitable for processing the predetermined task is predetermined; the resources available at a given point in time and/or a given event for the at least partial simultaneous configuration therein are determined, and the element group systems by which simultaneous processing is possible in a particularly efficient manner are selected from the predetermined number.

20. The method as recited in the preceding independent claim or a subclaim thereto,

wherein a first element group system is configured into the field; processing of the task is begun with this element group system until a preselected event occurs and task processing is continued thereafter in another element group system with at least partial reconfiguration.

21. The method as recited in the preceding independent claim or a subclaim thereto,
wherein the element group systems differ with regard to the processing speed, and the selection is made in response to the maximum achievable processing speed, also taking into account other aspects, if necessary.

22. A multidimensional processor field comprising a plurality of data processing cells arranged in proximity, having inputs that receive data from interconnection paths,
a logic unit gating these paths according to the particular function of their logic unit, and
outputs to output the gated data to interconnection paths,
wherein the data processing cells have an aspect ratio of at least 2:1, preferably 2:1.

23. The multidimensional processor field as recited in the preceding claim,
wherein the data processing cells are designed as coarsely granularly configurable cells.

24. The multidimensional processor field as recited in the preceding independent claim or a subclaim thereto,
wherein data processing cells are arranged in rows and columns.

25. The processor field as recited in the preceding claim,
wherein data inputs are provided in at least some of the

data processing cells to receive data from an upper row and data outputs are provided to output data to a lower row.

26. The processor field as recited in the preceding claim, wherein the data processing units are EALUs, ALUs and/or cells flanked by registers.

27. The method for configuring a processor field as recited in the preceding independent claim or a subclaim thereto, in which cells are selected for the configuration and their functions and interconnections are determined, an interconnection being determined in such a way that data is transmissible from cell to cell in a manner at least largely free of delay,
wherein cells not situated directly side by side but instead separated in width by a distance smaller than the length of the cell are also considered neighbor cells between which data is transmissible within one clock pulse or a low number of clock pulses.

28. A multidimensional processor field comprising a plurality of data processing cells situated in proximity, having inputs that receive data from interconnection paths,
a logic unit gating them according to the particular function of their logic unit, and
having outputs to output the gated data to interconnection paths,
wherein the data processing cells have an aspect ratio of at least 2:1, preferably 2:1.

29. The multidimensional processor field as recited in the preceding claim,
wherein the data processing cells are designed as coarsely granularly configurable cells.

30. The multidimensional processor field as recited in the preceding independent claim or a subclaim thereto, wherein data processing cells are arranged in rows and columns.

31. The processor field as recited in the preceding claim, wherein data inputs are provided in at least some of the data processing cells to receive data from an upper row and data outputs are provided to output data to a lower row.

32. The processor field as recited in the preceding claim, wherein the data processing units are EALUs, ALUs and/or cells flanked by registers.

33. The method for configuring a processor field as recited in the preceding independent claim or a subclaim thereto, in which cells are selected for configuration and their functions and interconnections are determined, an interconnection being determined in such a way that data is transmissible at least largely without delay from one cell to the next,
wherein cells not situated directly side-by-side but instead separated in width by a distance smaller than the length of the cell are also considered as neighbor cells between which data is transmissible within one clock pulse or a low number of clock pulses.

34. A data processing system having a multidimensional field of cell elements configurable in function and/or interconnection and
configuration maintenance means assigned thereto for local configuration maintenance,
wherein the configuration maintenance means are designed to maintain at least a portion of the maintained configurations in a nonvolatile form.

35. A data processing system having a multidimensional field of cell elements configurable in function and/or interconnection and
configuration maintenance means assigned thereto for local configuration maintenance,
wherein the configuration maintenance means are designed to maintain at least a portion of the maintained configurations in a nonvolatile form.

36. The data processing system as recited in the preceding independent claim or a subclaim thereto,
wherein the function is configurable in a coarsely granular form.

37. The data processing system as recited in the preceding independent claim or a subclaim thereto,
wherein the interconnection is configurable in a coarsely granular form.

38. The data processing system as recited in the preceding independent claim or a subclaim thereto,
wherein at least one of ALUs, EALUs, RAM cells, I/O cells, logic blocks are provided as cell elements.

39. The data processing system as recited in the preceding independent claim or a subclaim thereto,
wherein a separate configuration maintenance means is assigned to each cell element.

40. The data processing system as recited in the preceding independent claim or a subclaim thereto,
wherein the configuration maintenance means are designed to maintain a plurality of configurations.

41. A data processing system,
wherein multiple fixedly preselected nonvolatile

configurations are preselected in the configuration maintenance means.

42. The data processing system as recited in the preceding independent claim or a subclaim thereto, wherein the system is designed to use a variable configuration of a plurality of maintained configurations, in particular as wave reconfiguration or local sequencing.

43. The data processing system as recited in the preceding independent claim or a subclaim thereto, wherein configuration maintenance means that may be provided with variable configurations in runtime are provided in some cells.

44. The data processing system as recited in the preceding independent claim or a subclaim thereto, wherein at least one ROM, EPROM, EEPROM, flash memory, fuse- or antifuse-programmable memory means and/or in particular memory means fixedly provided in upper layers of a silicon structure are selected as the configuration maintenance means.

45. A method for manufacturing a dedicated data processing system,
wherein a multidimensional field having cell elements configurable in function and/or interconnection, and configuration maintenance means assigned thereto for local configuration maintenance are provided, a determination is made as to which configurations are to be maintained therein, and then nonvolatile configuration maintenance means are provided in such a way that they maintain at least a portion of the maintained configurations in nonvolatile form.

46. The method as recited in the preceding claim, wherein a multidimensional field that is runtime reconfigurable is assumed as the basis.

47. The method as recited in the preceding claim, wherein first a runtime reconfigurable multidimensional field having a reconfiguration circuit is assumed and then fields not necessary for reconfiguration are omitted.

48. A reconfigurable signal processing device having a plurality of signal processing circuits which may be linked together in particular in a configurable manner, their function being variable, and which have an output via which a reconfiguration is requested and/or acceptance of a reconfiguration may be provided, wherein at least a portion of the linkable signal processing circuits are analog signal processing circuits, and furthermore a reconfiguration unit is provided for preselecting configurations for the circuits that will process the analog signal.

49. The reconfigurable signal processing device as recited in the preceding claim, wherein some of the signal processing circuits are digital circuits.

50. A data processing device having a data processing logic cell field and at least one sequential CPU, wherein coupling of the sequential CPU and the data processing logic cell field for data exchange in blockwise form in particular is made possible through lines leading to a cache memory.

51. A method for dynamic setup of a connection between a sender and a receiver over one of a plurality of possible

paths leading from station to station,
wherein, starting from a unit (sender and/or receiver) which effects the bus setup, an inquiry is sent to the nearest stations that are ready for the bus setup,
a code number is assigned to these stations,
starting from at least a plurality, preferably from each free station which was assigned a code number, an inquiry is sent to the nearest stations inquiring as to the availability of the stations for a bus setup,
another code number is assigned to the available stations and this is continued until reaching the desired end of the bus.

52. The method as recited in the preceding claim,
wherein a modified code number is assigned from station to station, which is available for progress on the bus setup, regardless of whether or not the target is reached with this station.

53. The method as recited in the preceding claim,
wherein the change from station to station is comprehensibly selected, a count being incremented or decremented in particular by a fixed variable, in particular with a step size optionally through cyclic counting, i.e., counting in a finite cyclical numerical space.

54. The method as recited in the preceding claim,
wherein cyclical counting is performed up to at least three different numerical values to characterize the station.

55. The method as recited in the preceding independent claim or a subclaim thereto,
wherein after setup of a bus path between the sender and receiver, stations not needed are freed again.

56. The method as recited in the preceding independent claim or a subclaim thereto,
wherein a bus is considered as having been set up as soon as the target has been reached from a station.

57. The method as recited in the preceding claim,
wherein the setup of additional bus connections is suppressed after setup of a first bus.

58. The method as recited in the preceding claim,
wherein the stations that have participated in setting up a bus are notified that the bus setup has been achieved.

59. The method as recited in the preceding claim,
wherein the stations that have participated in setting up a bus are notified that the bus setup has been achieved; this is done by sending a bus sharing signal in the reverse direction to the stations that shared in the bus, starting from the target, in particular by transmitting signals along the bus.

60. The method as recited in the preceding claim,
wherein the stations that have participated in setting up the bus are identified by comparing the numerical values which may have been assigned, to the reachable stations, starting from the target, and the stations having a numerical value indicative of belonging to a bus are selected.

61. The method as recited in the preceding claim,
wherein the numerical values are incremented starting from a starting position, whereas in bus setup, progress goes from one station to the next and after reaching the target the stations having the smallest numerical values of reachable stations are identified as belonging to the bus.

62. The method as recited in the preceding claim, wherein stations not needed for a bus connection are freed by marking the stations that have participated in a needed bus setup, and by freeing all stations not marked in this way in particular by sending a global release signal.

63. The method as recited in the preceding independent claim or a subclaim thereto, wherein the release of stations that are not needed takes place in waves by running back from a target unit to a starting unit and/or by running backward from the target to the start with the release of stations that are not needed by sending a release signal through the station that had inquired previously with the station to be freed as to whether it is available for setting up the bus.

64. The method as recited in the preceding independent claim or a subclaim thereto, a plurality of bus connections being set up simultaneously, wherein a directional value is assigned to each station addressed for setting up a bus connection, in particular being stored in the station, indicating from which direction or from which station being addressed a bus setup request signal has been obtained.

65. The method as recited in the preceding claim, wherein the bus verification is performed by analyzing the signals which indicate from which addressing station a bus setup request signal has been sent and in which the bus setup toward this requesting station takes place.

66. The method as recited in the preceding independent claim or a subclaim thereto, wherein, when there are multiple buses, requiring an equal number of stations, which are potentially able to

be set up, a bus is selected on the basis of an evaluation criterion that may be and/or has been assigned to the bus.

67. The method as recited in the preceding claim, wherein the number of stations running through horizontally and/or vertically and/or the number of stations having registers and/or the connection density of existing bus connections along the stations and/or the size of remaining free fields not distributed by the bus is used as a bus evaluation criterion.

68. A multidimensional field of reconfigurable elements in which buses that can be set up dynamically are provided at least between some of the configurable elements, wherein units provided in the bus system are designed to address neighbor groups in bus segments either directly or indirectly via bus networks and/or to store a bus station number and/or to store a request signal direction and/or to permit, through release, temporary connections to be broken up wherever possible for stations needed for bus setup after determining the lack of need.

69. A data processing device having a data processing logic cell field and at least one sequential CPU, wherein coupling of the sequential CPU and the data processing logic cell field for data exchange in blockwise form in particular is made possible through lines leading to a cache memory.